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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/601,937

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Jae-Sun Yun

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7804

20792

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08/12/2004

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EXAMINER

PERKINS, PAMELA E

ART UNIT

PAPER NUMBER

2822

DATE MAILED: 08/12/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/601,937

Applicant(s)

YUN ET AL.

Examiner

Pamela E Perkins

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 24 June 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) 7-10 is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-6 and 11-20 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 24 June 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_.
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_.

### **DETAILED ACTION**

This office action is in response to the filing of the application papers on 24 June 2003. Claims 1-20 are pending; claims 7-10 have been withdrawn from consideration.

### ***Election/Restrictions***

Restriction to one of the following inventions is required under 35 U.S.C. 121:

- I. Claims 1-6 and 11-20, drawn to a method of manufacturing a semiconductor device, classified in class 438, subclass 437.
- II. Claims 7-10, drawn to a semiconductor device, classified in class 257, subclass 374.

The inventions are distinct, each from the other because of the following reasons:

Inventions I and II are related as process of making and product made. The inventions are distinct if either or both of the following can be shown: (1) that the process as claimed can be used to make other and materially different product or (2) that the product as claimed can be made by another and materially different process (MPEP § 806.05(f)). In the instant case the product as claimed can be made by another and materially different process. For example, the product as claimed discloses a recessed conformal liner layer, the recessed conformal liner layer may be formed by ashing or planarization rather than etching as required by the process as claimed.

Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, restriction for examination purposes as indicated is proper.

Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a request under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

During a telephone conversation with Robert Crouse on 19 July 2204 a provisional election was made without traverse to prosecute the invention of group 1 drawn to a method of manufacturing a semiconductor device, claims 1-6 and 11-20. Affirmation of this election must be made by applicant in replying to this Office action. Claims 7-10 are withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

### ***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1 and 4-6 are rejected under 35 U.S.C. 102(e) as being anticipated by Knorr et al. (6,531,377).

Knorr et al. disclose a method of forming a trench isolated integrated circuit device where a buffer insulation layer (122) and a hard mask layer (114) are formed on an integrated circuit substrate (112); forming an opening in the hard mask layer (114) and in the buffer layer (122) to expose the integrated circuit substrate (112) (col. 4, lines 3-9); forming a trench (111) including sidewalls in the integrated circuit substrate (112) that is exposed by the opening; forming a sidewall oxide layer (121) on the sidewalls of the trench (111); forming a conformal liner layer (125) on the sidewall oxide layer (121); forming a lower device isolation layer (116, 126) in the trench (111) and extending onto the trench sidewalls, the lower device isolation layer (116, 126) including grooves therein, a respective one of which extends along a respective one of the sidewalls (col. 4, lines 10-63); forming an upper device isolation layer (230) on the lower device isolation layer (116, 126) and in the grooves (col. 5, line 63 thru col. 6, line 21); removing the hard mask layer (114) (col. 6, lines 6-22), such that the grooves extend a predetermined depth from the substrate face; and forming a plurality of transistors on the trench isolated integrated circuit device (col. 1, lines 18-32). Knorr et al. further disclose the lower device insulation layer (116, 126) comprising a first insulation layer (116) on the conformal liner layer (125); and forming a second insulation layer (126) on the first insulation layer (116) (col. 4, line 64 thru col. 5, line 45).

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

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(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 2, 3, 11-13, 15, 16 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Knorr et al. in view of Chen et al. (6,093,600).

Knorr et al. disclose the subject matter claimed above except etching the conformal liner layer to recess the conformal liner layer relative to the lower device insulation layer adjacent thereto, to thereby defining the grooves and removing the buffer insulation layer.

Chen et al. disclose a method of forming a trench isolated integrated circuit device where a buffer insulation layer (102) and a hard mask layer (104) are formed on an integrated circuit substrate (100); forming an opening in the hard mask layer (104) and in the buffer layer (102) to expose the integrated circuit substrate (100); forming a trench (106) including sidewalls in the integrated circuit substrate (100) that is exposed by the opening; forming a sidewall oxide layer (108) on the sidewalls of the trench (106); forming a conformal liner layer (110) on the sidewall oxide layer (108) (col. 3, lines 18-33); forming a device isolation layer (112) in the trench (106) and extending onto the trench sidewalls; removing the hard mask layer (104) and the buffer insulation layer (102), such that the grooves extend a predetermined depth from the substrate face; and forming a plurality of transistors (116) on the trench isolated integrated circuit device (col. 3, lines 33-64). Chen et al. further disclose etching the conformal liner layer (110) to recess the conformal liner layer (110) relative to the device insulation layer (112)

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adjacent thereto, to thereby defining the grooves (114) (Fig. 1E; col. 3, line 65 thru col. 4, line 21).

Since Knorr et al. and Chen et al. are both from the same field of endeavor, a method of forming a trench isolated integrated circuit device, the purpose disclosed by Chen et al. would have been recognized in the pertinent art of Knorr et al. Therefore, it would have been obvious to one ordinary skill in the art at the time the invention was made to modify Knorr et al. by etching the conformal liner layer to recess the conformal liner layer relative to the device insulation layer adjacent thereto, to thereby defining the grooves as taught by Chen et al. to decrease the aspect ratio and increase reliability (col. 1, lines 48-62).

Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Knorr et al. in view of Chen et al. as applied to claim 11 above, and further in view of Hung et al. (6,750,117).

Knorr et al. in view of Chen disclose the subject matter claimed above except forming a conformal etch protection layer on the conformal liner layer prior to forming the lower device insulation layer.

Hung et al. disclose a method of forming a trench isolated integrated circuit device where a buffer insulation layer (210) and a hard mask layer (220) are formed on an integrated circuit substrate (200); forming an opening in the hard mask layer (220) and in the buffer layer (210) to expose the integrated circuit substrate (200); forming a trench (230) including sidewalls in the integrated circuit substrate (200) that is exposed by the opening 9col. 2, lines 47-65); forming a sidewall oxide layer (233) on the

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sidewalls of the trench (230); forming a conformal liner layer (240) on the sidewall oxide layer (233); a conformal etch protection layer (247) on the conformal liner layer (240); forming a device isolation layer (250) in the trench (230) and extending onto the trench sidewalls (col. 2, line 66 thru col. 3, line 28); and removing the hard mask layer (220) and the buffer insulation layer (210) (col. 3, lines 29-39).

Since Knorr et al. and Hung et al. are both from the same field of endeavor, a method of forming a trench isolated integrated circuit device, the purpose disclosed by Hung et al. would have been recognized in the pertinent art of Knorr et al. Therefore, it would have been obvious to one ordinary skill in the art at the time the invention was made to modify Knorr et al. by forming a conformal etch protection layer on the conformal liner layer prior to forming the device insulation layer as taught by Hung et al. to reduce leakage (col. 1, lines 33-45).

Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Knorr et al. in view of Chen et al. as applied to claim 11 above, and further in view of Lim et al. (6,65,302).

Knorr et al. in view of Chen et al. disclose the subject matter claimed above except conformally forming a capping insulation layer to fill the groove, wherein the capping insulation layer comprises insulation material having an etch selectivity with respect to the hard mask layer.

Lim et al. disclose a method of forming a trench isolated integrated circuit device where a buffer insulation layer (4) and a hard mask layer (6) are formed on an integrated circuit substrate (2); forming an opening in the hard mask layer (6) and in the



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buffer layer (4) to expose the integrated circuit substrate (2); forming a trench (8) including sidewalls in the integrated circuit substrate (2) that is exposed by the opening; forming a lower device isolation layer (26) in the trench (8) and extending onto the trench sidewalls, the lower device isolation layer (26) including grooves therein, a respective one of which extends along a respective one of the sidewalls (col. 5, line 38 thru col. 6, line 25); forming an upper device isolation layer (24) on the lower device isolation layer (26) and in the grooves; removing the hard mask layer (6) and the buffer insulation layer (4) (col. 6, lines 26-59); and forming a plurality of transistors on the trench isolated integrated circuit device (col. 1, lines 17-52). Lim et al. further disclose conformally forming a capping insulation layer (22) to fill the groove, wherein the capping insulation layer (22) comprises insulation material having an etch selectivity with respect to the hard mask layer (6) (col. 6, lines 14-59).

Since Knorr et al. and Lim et al. are both from the same field of endeavor, a method of forming a trench isolated integrated circuit device, the purpose disclosed by Lim et al. would have been recognized in the pertinent art of Knorr et al. Therefore, it would have been obvious to one ordinary skill in the art at the time the invention was made to modify Knorr et al. by conformally forming a capping insulation layer to fill the groove, wherein the capping insulation layer comprises insulation material having etch selectivity with respect to the hard mask layer as taught by Lim et al. to improve planarization (col. 3, lines 10-41).

Claims 18 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Knorr et al. in view of Chen et al. as applied to claim 11 above, and further in view of Shin et al. (6,624,464).

Knorr et al. in view of Chen et al. disclose the subject matter claimed above except sequentially forming a tunnel insulation layer, a first floating gate conductive layer, a buffer insulation layer, and a hard mask layer on a substrate face; successively patterning the hard mask layer, the buffer insulation layer, the first floating gate conductive layer, and the tunnel insulation layer to form a first floating gate pattern and an opening that exposes a predetermined region of the substrate; and wherein the etching comprises etching the hard mask layer and the buffer insulation layer until the first floating gate pattern is exposed; forming a second floating gate pattern on the first floating gate pattern; sequentially forming a dielectric layer and a control gate conductive layer on the substrate face and the second floating gate pattern; and successively etching the control gate conductive layer, the dielectric layer, the second floating gate pattern and the first floating gate pattern to form a first floating gate electrode, a second floating gate electrode, a dielectric pattern and a control gate electrode.

Shin et al. disclose a method of forming a trench isolated integrated circuit device where a tunnel insulation layer (520), a first floating gate conductive layer (530), a buffer insulation layer (532), and a hard mask layer (534) are formed on a substrate face (500); successively patterning the hard mask layer (534), the buffer insulation layer (532), the first floating gate conductive layer (530), and the tunnel insulation layer (520)

to form a first floating gate pattern and an opening that exposes a predetermined region of the substrate (500); forming a trench including sidewalls in the substrate (500) that is exposed by the opening; forming a device isolation layer (510) in the trench and extending onto the trench sidewalls; and removing the hard mask layer (534) and the buffer insulation layer (532) (col. 5, line 56 thru col. 6, line 18). Shin et al. further disclose forming a second floating gate pattern (540) on the first floating gate pattern (530); sequentially forming a dielectric layer (550) and a control gate conductive layer (580) on the substrate face (500); and successively etching the control gate conductive layer (580), the dielectric layer (550), the second floating gate pattern (540) and the first floating gate pattern (530) to form a first floating gate electrode, a second floating gate electrode, a dielectric pattern and a control gate electrode (col. 6, lines 18-65).

Since Knorr et al. and Shin et al. are both from the same field of endeavor, a method of forming a trench isolated integrated circuit device, the purpose disclosed by Shin et al. would have been recognized in the pertinent art of Knorr et al. Therefore, it would have been obvious to one ordinary skill in the art at the time the invention was made to modify Knorr et al. by sequentially forming a tunnel insulation layer, a first floating gate conductive layer, a buffer insulation layer, and a hard mask layer on a substrate face; successively patterning the hard mask layer, the buffer insulation layer, the first floating gate conductive layer, and the tunnel insulation layer to form a first floating gate pattern and an opening that exposes a predetermined region of the substrate; and wherein the etching comprises etching the hard mask layer and the buffer insulation layer until the first floating gate pattern is exposed; forming a second

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floating gate pattern on the first floating gate pattern; sequentially forming a dielectric layer and a control gate conductive layer on the substrate face and the second floating gate pattern; and successively etching the control gate conductive layer, the dielectric layer, the second floating gate pattern and the first floating gate pattern to form a first floating gate electrode, a second floating gate electrode, a dielectric pattern and a control gate electrode as taught by Shin et al. to prevent errors in the etching process (col. 2, lines 46-65).

### ***Conclusion***


Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pamela E Perkins whose telephone number is (571) 272-1840. The examiner can normally be reached on Monday thru Friday, 9:00am to 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (571) 272-1852. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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